

SMART
Embedded
Products

Product Specification

**SMART MODULAR
microSD™ MEMORY CARDS
1GB and 2GB SDSC Memory Cards
4GB SDHC Memory Cards**

SH9UDxxxGPHF9Sx11

April 2015, RevA



www.smartm.com

REVISION HISTORY

Date	Revision	Section(s)	Description
April 2015	A	All	Initial release



ESD Caution – Handling

Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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1. GENERAL DESCRIPTION

1.1 Overview

SMART is a leading independent manufacturer of memory and embedded modular sub-systems inclusive of board-level through systems level design, manufacturing, test, and fulfillment services. We offer more than 500 standard and custom products to leading OEMs in the computer, industrial, networking and telecommunications industries worldwide.

SMART's v3.0 Micro Secure Digital (microSD) card is fully compliant with the SD Card Association specification. The Command List complies with Part 1 Physical Layer Specification v3.01 final definitions, Card Capacity of Non-secure Area, and v3.00 of the Secure Area Part 3 Security Specification.

The microSD card comes with 8-pin interface, designed to operate at a maximum operating frequency of 50MHz or 100MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption.

SMART's microSD card is suitable for hand-held applications in semi-industrial/medical markets and is one of the most popular cards today based on its high performance, good reliability and wide compatibility.

SMART has built its foundation by providing proven technology and quality products to the most demanding Fortune 100 OEMs. SMART engineers its products to perform at the highest degree of reliability & compatibility while backing these products with outstanding services and technology expertise.

About SMART

SMART is a leading independent manufacturer of memory and embedded modular sub-systems inclusive of board-level through system-level design, manufacturing, test, and fulfillment services. We offer more than 500 standard and custom products to leading OEMs in the computer, industrial, networking and telecommunications industries worldwide.

1.2 Features

- **Form Factor:** microSD
- **Interface:** Industry standard SD [Part 1 Physical Layer Specification Ver3.01 Final]
- **Supports SD SPI Mode**
- **Bus Widths Supported:** x1 and x4
- **Supported Bus Speed Modes** (using x4 bus width)
 - **Default Speed Mode:** 3.3 V signaling, up to 25 MHz, up to 12.5 MB/s
 - **High Speed Mode:** 3.3 V signaling, up to 50 MHz, up to 25 MB/s
 - **SDR12:** 1.8 V signaling, up to 25 MHz SDR, up to 12.5 MB/s
 - **SDR25:** 1.8 V signaling, up to 50 MHz SDR, up to 25 MB/s
 - **SDR50:** 1.8 V signaling, up to 100 MHz SDR, up to 50 MB/s
 - **SDR104:** 1.8 V signaling, up to 208 MHz SDR, up to 104 MB/s
 - **DDR50:** 1.8 V signaling, up to 50 MHz DDR, up to 50 MB/s
- 1. NOTE: Timing varies between UHS-I (1.8 V) and Standard (3.3 V) signaling
- **NAND Technology:** Single Level Cell (SLC)
- **Capacity:**
 - SDSC: 1 and 2 GBytes
 - SDHC: 4 GBytes
- **Low Power Dissipation:**
 - **Read:** 110 mA
 - **Write:** 110 mA
- **Operating Temperature:**
 - **Extended:** -25°C to +85°C
 - **Industrial:** -40°C to +85°C
- **Input Power:** 2.7 V – 3.6 V
- **Dimensions:** 15 mm(L) x 11 mm(W) x 1 mm(H)
- **ESD protection:** +4 kV/-4 kV in contact pads

1.3 Unique Features

- Implements Global Static and Dynamic Wear Leveling for longer life
- Supports Advanced Error Detection/Correction for superior data reliability
- Device health information (erase count, bad block and spare count) is available via vendor specific command (Application Note available upon request)
- Command list supports [Part 1 Physical Layer Specification Ver3.01 Final] definitions
- Copyright Protection Mechanism: fully-compliant to the highest security SDMI Standard
- Supports CPRM (Content Protection for Recordable Media) for recorded content
- Power Loss Protection
- Password Protection of cards (optional)
- Provides a mechanical switch for Write Protection
- Built-in write protection features (permanent and temporary)
- RoHS compliant and Low Halogen

2. OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

2.1 Performance

Table 1: Performance Characteristics

Item	Bus Configuration	Capacity	Performance ¹ (MB/s)
Sequential Read	Default (3.3 V, 25 MHz)	All	21
	High Speed (3.3 V, 50 MHz)	All	21
	SDR12 (1.8V, 25MHz)	4 GB ²	21
	SDR25 (1.8V, 50MHz)	4 GB ²	21
	SDR50 (UHS-I, 1.8V, 100MHz)	4 GB ²	21
	SDR104 (UHS-I, 1.8V, 208MHz)	4 GB ²	21
	DDR50 (UHS-I, 1.8V, 50MHz)	4 GB ²	21
Sequential Write	Default (3.3V, 25MHz)	All	15
	High Speed (3.3V, 50MHz)	All	18
	SDR12 (1.8V, 25MHz)	4 GB ²	18
	SDR25 (1.8V, 50MHz)	4 GB ²	18
	SDR50 (UHS-I, 1.8V, 100MHz)	4 GB ²	18
	SDR104 (UHS-I, 1.8V, 208MHz)	4 GB ²	18
	DDR50 (UHS-I, 1.8V, 50MHz)	4 GB ²	18

1. Performance measured using Testmetrix VTE-4100.
2. Only 4 GB drives support these speeds.

2.2 Power

Table 2: Power Requirements

Parameter	Symbol	Minimum	Typical	Maximum	Units	
Supply Voltage	VCC	2.7	3.3	3.6	V	
Operating Current	I _{CC1}	-	1GB/2GB	90	100	mA
			4GB	190	200	
Standby Current	I _{CC1}	-	1GB/2GB	140	150	μA
			4GB	240	250	
Input Leakage Current	I _{LI}	-10	-	10	μA	
Output Leakage Current	I _{LO}	-10	-	10	μA	

2.3 Reliability

Table 3: Reliability Characteristics

Item	Value
Mean Time Between Failures (MTBF)	> 3 Million hours
Data Reliability	< 1 Non-Recoverable Error in 10 ¹⁴ bits read
Data Retention (@ 40°C)	10 years > 90% life remaining
	1 year < 10% life remaining
Endurance ¹	SLC: 6 TBytes per 1 GB card capacity
Error Correction / Error Detection	Up to 24 bits for every 1 Kbyte of user data

2.4 Endurance

- **Static & Dynamic Wear Leveling:** This feature eliminates overstressing flash media by spreading the data writes across all flash physical address space, including logical areas that are not written by the user. The data is wear leveled across the entire drive.
- **ECC:** microSD XL products utilize BCH ECC to provide correction of up to 24 random single-bit errors per 1 Kbyte of user data.
- **Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of flash media and replaces them with new ones from the spare pool.

2.5 Mean Time Between Failures (MTBF)

SMART Modular Technology has derived the following reliability statistics using **Telcordia SR-332, Issue 2 - Parts Count Method** and based upon numerous specifics related to and including: internal component packaging, pin configurations, component density, and internal component substrate architecture. Product reliability modeling for SMART Modular Technology is based upon continual usage of the product, within accepted normal operating parameters. Compromise of the published normal operating parameters will adversely affect the product life-span reliability model.

Table 4: MTBF Values - Telcordia SR-332, Issue 2 - Parts Count Method at 50°C

Drive	MTBF (Hours)
All Capacities	> 3 Million hours

2.6 Environmental Conditions

Table 5: Environmental Conditions and Test Conditions

Parameter	Value
Shock - (Non-Operating Industrial microSD)	1500g max @ 0.5 ms Half-Sine Pulse Duration
Vibration - (Non-Operating Industrial microSD)	Frequency/Displacement: 20Hz~80Hz/1.52mm Frequency Acceleration: 80Hz~2000Hz/20G Vibration Orientation: X, Y, Z axis/30 min for each
Operating Temperature - Extended	-25°C to +85°C
Operating Temperature - Industrial	-40°C to +85°C
Humidity	0% to 95%

2.7 Physical Characteristics

Table 6: Physical Characteristics

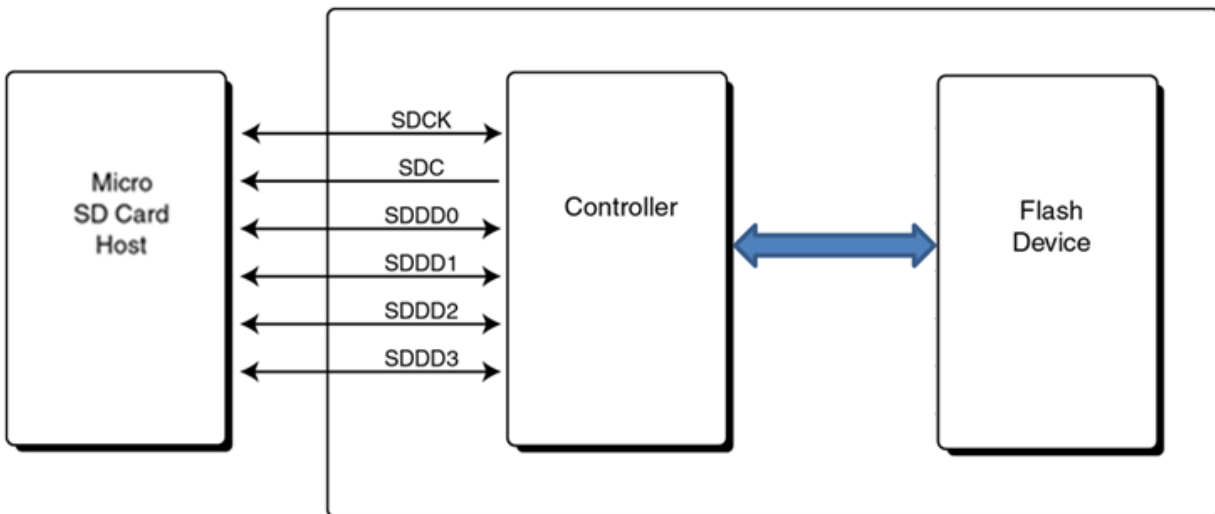
Parameter	Value
Length	15.0 mm [0.590 in]
Width	11.0 mm [0.433 in]
Thickness	1.0 mm [0.039 in]
Weight	0.4 g [0.014 oz]

3. PRODUCT DESCRIPTION

SMART's Micro Secure Digital (microSD) Memory Card product line is offered in a UL approved housing with an advanced 8-pin connector. It contains a controller and a flash memory device. The on-board controller interfaces with a microSD Card Host allowing data to be written to and read from the flash memory device.

3.1 Functional Block Diagram

Figure 1: microSD XL Block Diagram



4. REGULATORY COMPLIANCE

The SMART Modular XL microSD product complies with the regulatory requirements identified in the following table.

Table 7: Regulatory Description

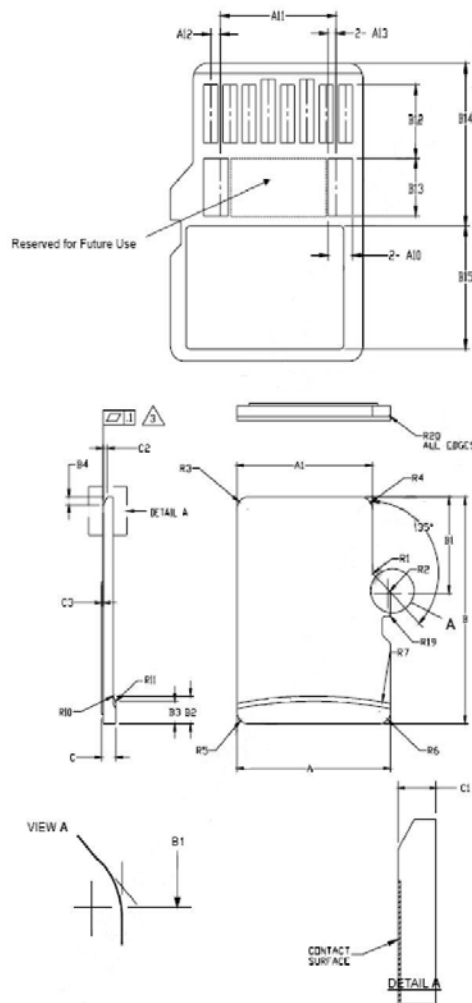
Regulation	Compliance (Country/Region)
EMC	FCC Part 15, Class B (USA); IC ICES-003, Class B (Canada); EMC Directive 2004/108/EC - EN 55022, Class B and EN 55024 (EU), CISPR 22, Class B and CISPR 24 (International)
RoHS	RoHS Directive 2011/65/EU - EN 50581 (EU)



5. MECHANICAL SPECIFICATION

5.1 Mechanical Dimensions

Figure 2: microSD XL Dimensions




COMMON DIMENSIONS				
SYMBOL	MIN	NCM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2. DIMENSIONS ARE IN MILLIMETERS.

 COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

6. ELECTRICAL SPECIFICATION

6.1 Electrical Interface

The SMART microSD Memory Cards are fully compliant with the Secure Digital specification (V1.1 and V1.01). The following table describes the I/O signals of the card. Signals whose source is the Host are designated as inputs (I) while signals that the microSD card sources are outputs (O). Bi-directional signals are designated as Input/Output (I/O) or Input/Output using push-pull drivers (PP).

Table 8: Pinout Assignments and Pin Types

Pin	Signal Name	Type	Signal Description
1	DAT2	I/O / PP	Data Line [bit2]
2	CD/DAT3	I/O / PP	Card Detect / Data Line [bit1]
3	CMD	PP	Command / Response
4	VCC	S	Supply Voltage
5	CLK	I	Clock
6	GND	S	Supply Voltage Ground
7	DAT0	I/O / PP	Data Line [bit0]
8	DAT1	I/O / PP	Data Line [bit1]

6.2 Absolute Maximum Ratings

Table 9: Absolute Maximum Ratings¹

Symbol	Parameter	MIN	MAX	Unit
$V_{DD}-V_{SS}$	DC Power Supply	-0.3	+3.3	V
V_{IN}	Input Voltage	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
T_a	Operating Temperature (Commercial)	0	+70	°C
T_a	Operating Temperature (Extended)	-25	+85	°C
T_a	Operating Temperature (Industrial)	-40	+85	°C
T_{st}	Storage Temperature	-40	+85	°C
V_{DD}	V_{DD} Voltage	2.7	3.6	V

1. Stress beyond the Absolute Maximum Rating conditions may result in permanent damage to the device. These are stress ratings only and functional operation should be restricted to those indicated in the operational sections of this specification. Exposure to conditions beyond recommended, up to and including the Absolute Maximum Rating conditions, for extended periods may affect device reliability.

7. POWER CYCLING

7.1 Power On or Power Cycle

To assure reliable SD Card hard reset the following requirements must be met:

- Voltage level shall be below 0.5V.
- Duration shall be at least 1ms.

7.2 Power Supply Ramp Up

The power ramp-up time is defined from the 0.5 V threshold level up to the operating supply voltage, which must be stable between VDD (2.7 V) and VDD (max). The following recommendations are made concerning power ramp up:

- Ramp voltage should be monotonic as much as possible.
- The minimum ramp up time should be 0.1 ms.
- The maximum ramp up time should be 35 ms for 2.7 - 3.6 V power supply.

7.3 Power Down and cycle

When the host shuts down the power, the card VDD shall be lowered to less than 0.5V for a minimum period of 1 ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logic 0 (zero) level by the host to avoid a situation that the operating current is drawn through the signal lines.

If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State*. To create a power cycle the host shall follow the power down description before powering up the card (i.e. the card VDD shall be once lowered to less than 0.5 V for a minimum period of 1 ms).

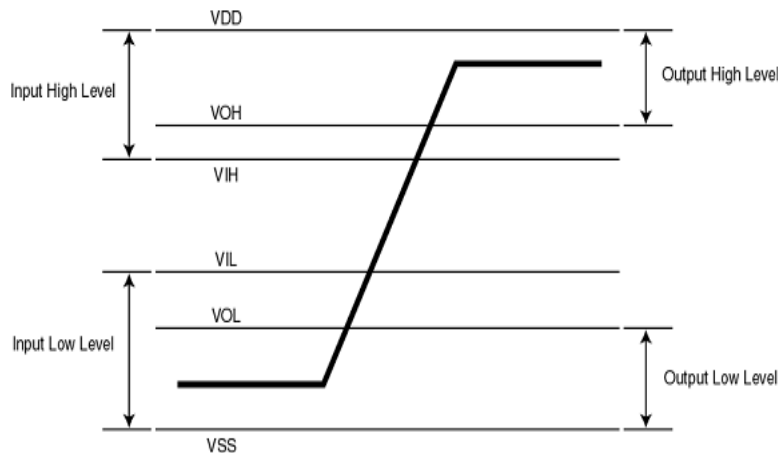
8. DC CHARACTERISTICS

8.1 Bus Signal Line Levels

Table 10: Bus Signal Line Levels

Symbol	Parameter	Ratings	Unit
R_{CMD}	Pull-up Resistor value for SDC Line	10 – 100	k Ω
R_{DAT}	Pull-up Resistor value for SDD Line	10 – 100	k Ω
C_L	Bus Line Capacitance	40	pF
CCARD	Capacitance of the card for each signal pin	10 (max)	pF
L_{SI}	Signal Line Inductance	16	nH
RDAT3	Pull-up resistance inside card (pin1)	10 - 90	k Ω

Figure 3: Bus Signal Level



8.2 Bus Operation Conditions for 3.3 V Signaling

Table 11: Threshold Level for High Voltage Range

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	2.7	3.6	V
V_{OH}	Output High Voltage	$0.75 \cdot V_{CC}$	-	V
V_{OL}	Output Low Voltage	-	$0.125 \cdot V_{CC}$	V
V_{IH}	Input High Voltage	$0.625 \cdot V_{CC}$	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{SS} - 0.3$	$0.25 \cdot V_{CC}$	V
t_{PUP}	Power Up Time (0 V to V_{DD} min)	-	250	ms

9. AC CHARACTERISTICS

9.1 Interface timing (Default Mode)

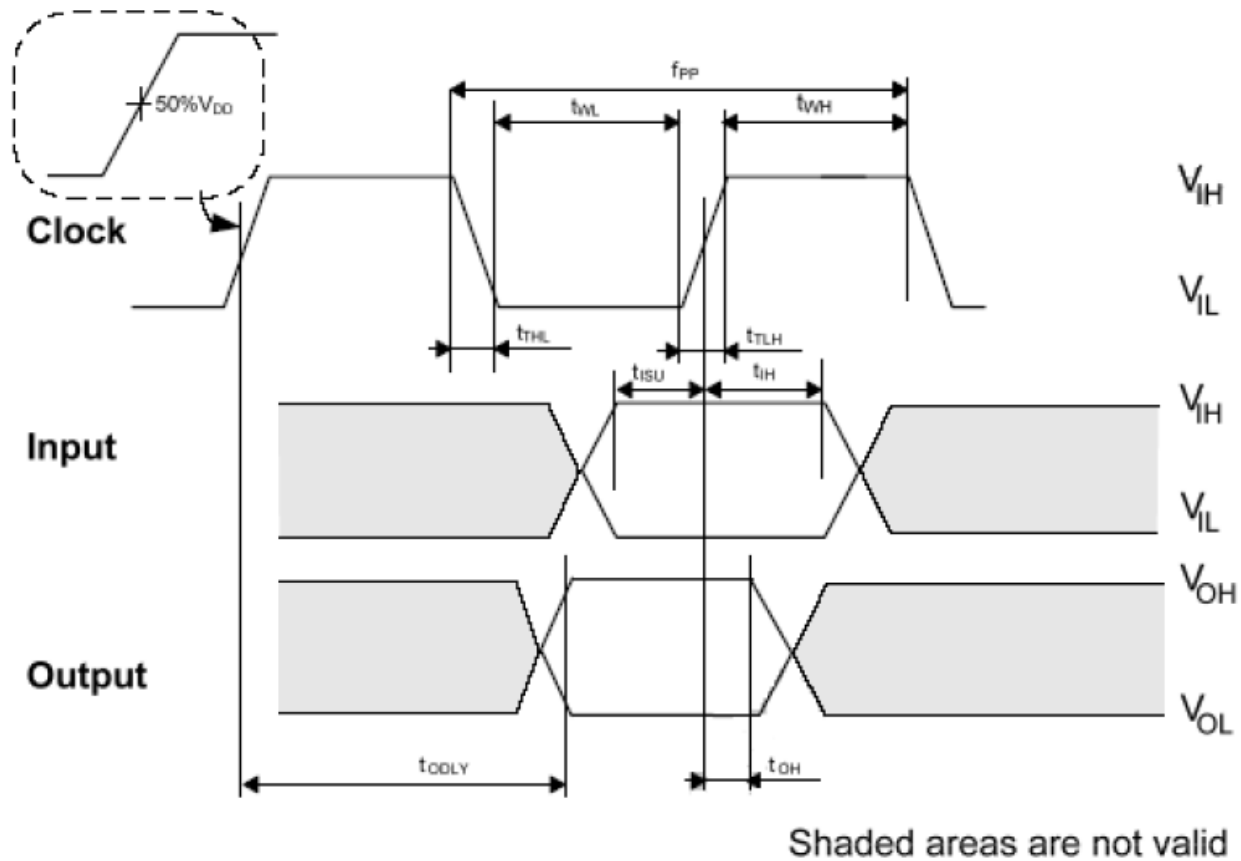


Table 12: Bus Timing (Default Mode)

Symbol	Parameter	Min	Max	Unit	Remark
f_{PP}	Clock frequency data transfer mode	0	25	MHz	$C_L \leq 10$ pF
t_{OD}	Clock frequency identification mode	0	400	kHz	$C_L \leq 10$ pF
t_{WL}	Clock low time	10	-	ns	$C_L \leq 10$ pF
t_{WH}	Clock high time	10	-	ns	$C_L \leq 10$ pF
t_{TLH}	Clock rise time	-	10	ns	$C_L \leq 10$ pF
t_{THL}	Clock fall time	-	10	ns	$C_L \leq 10$ pF
t_{ISU}	Input setup time	5	-	ns	$C_L \leq 10$ pF
t_{IH}	Input hold time	5	-	ns	$C_L \leq 10$ pF
$t_{OLDY-tran}$	Output delay time (Data Transfer Mode)	0	14	ns	$C_L \leq 10$ pF
$t_{OLDY-ident}$	Output delay time (Identification Mode)	0	50	ns	$C_L \leq 10$ pF

9.2 Interface Timing (High Speed Mode)

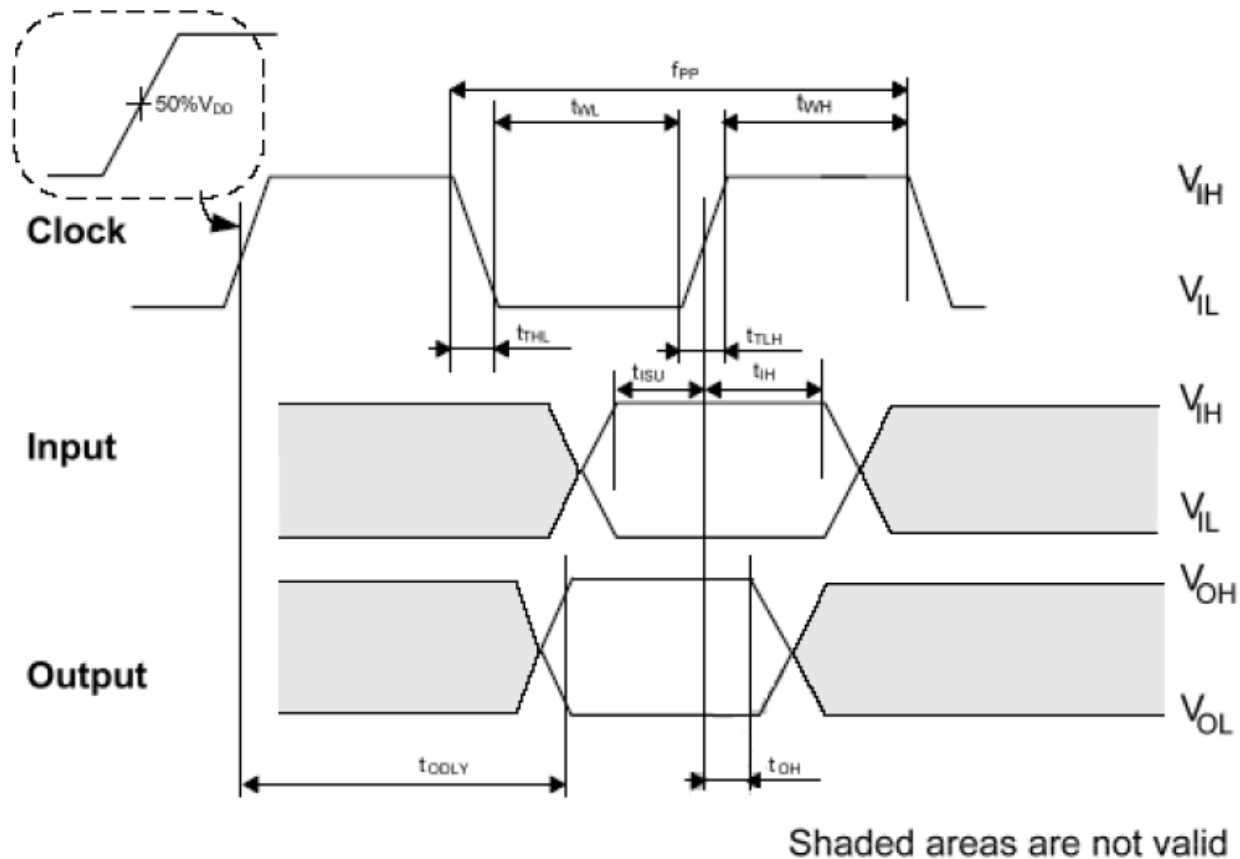


Table 13: Bus Timing (High Speed Mode)

Symbol	Parameter	Min	Max	Unit	Remark
f _{PP}	Clock frequency data transfer mode	0	50	MHz	C _L ≤ 10 pF
t _{WL}	Clock low time	7		ns	C _L ≤ 10 pF
t _{WH}	Clock high time	7		ns	C _L ≤ 10 pF
t _{TLH}	Clock rise time		3	ns	C _L ≤ 10 pF
t _{THL}	Clock fall time		3	ns	C _L ≤ 10 pF
t _{ISU}	Input setup time	6		ns	C _L ≤ 10 pF
t _{IH}	Input hold time	2		ns	C _L ≤ 10 pF
t _{OLDY}	Output delay time		14	ns	C _L ≤ 10 pF
t _{OH}	Output hold time	2.5	50	ns	C _L ≤ 10 pF

10. REGISTERS

The supported microSD registers used in the SMART MicroSD cards are shown in Table 12. CID, RCA, CSD, SDR, and OCR registers are described in detail in the sections that follow.

Table 14: Supported microSD Registers

Name	Width	Description
CID	128	Card Identification
RCA	16	Relative Card Address
DSR	16	Driver Stage Register
CSD	128	Card Specific Data
SCR	64	SD Configuration Register
OCR	32	Operation Condition Register
SSR	512	SD Status Register

10.1 Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the information used during the card identification phase. Every individual flash card will have a unique identification number. The fields for the CID register are presented in the following table.

Table 15: Card Identification Register (CID) Fields

Bits	Width	Name	Field	Value
[127:120]	8	Manufacturer ID	MID	0x27
[119:104]	16	OEM/Application ID	OID	0x5048
[103:64]	40	Product Name	PNM	SDXXG ⁽¹⁾
[63:56]	8	Product Revision	PRV	3.0 (0x30) ⁽²⁾
[55:24]	32	Product Serial Number	PSN	-- ⁽³⁾
[23:20]	4	Reserved	--	--
[19:8]	12	Manufacturing Date	MDT	-- ⁽³⁾
[7:1]	7	CRC7 Checksum	CRC	-- ⁽³⁾
[0]	1	Not used, Always 1	-	1b

- (1) XX is the drive capacity: 01, 02, 04.
- (2) Support SD 3.0 spec, 0x30
- (3) Defined by the Card Initialization Tool

10.2 Relative Card Address (RCA)

The Relative Card Address (RCA) register is 16 bits wide. It contains the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the identification procedure. The default value of the RCA register is 0x0000.

10.3 Driver Stage Register (DSR) – Optional

The 16-bit Driver Stage Register (DSR) can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

10.4 Card Specific Data (CSD)

The Card Specific Data (CSD) register is 128 bits wide. It provides information on how to access the card contents. The fields for the CSD register are presented in the following table.

Table 16: Card Specific Data (CSD) Fields (1GB/2GB SDSC)

Bits	Width	Name	Field	Value
[127:126]	2	CSD Structure	CSD_STRUCTURE	00b
[125:120]	6	Reserved	---	00 0000b
[119:112]	8	Data Read Access Time 1	TAAC	5Eh
[111:104]	8	Data Read Access Time 2	NSAC	00h
[103:96]	8	Max. Bus Clock Frequency	TRAN_SPEED	32h ⁽¹⁾
[95:84]	12	Card Command Classes	CCC	5B5h ⁽²⁾
[83:80]	4	Max Read Block Data Length	READ_BLK_LEN	9h ^{1GB} Ah ^{2GB}
[79]	1	Partial Block Read Allowed	READ_BLK_PARTIAL	1b
[78]	1	Write Block Misalignment	WRITE_BLK_MISALIGN	0b
[77]	1	Read Block Misalignment	READ_BLK_MISALIGN	1b
[76]	1	DSR implemented	DSR_IMP	0b
[75:74]	2	Reserved	---	---
[73:62]	12	Device Size	C_SIZE	-- ⁽³⁾
[61:59]	3	Max R_current @ VDD min	VDD_R_CURR_MIN	111b (100 mA)
[58:56]	3	Max R current @ VDD max	VDD_R_CURR_MAX	111b (200 mA)
[55:53]	3	Max W_current @ VDD min	VDD_W_CURR_MIN	111b (100 mA)
[52:50]	3	Max W current @ VDD max	VDD_W_CURR_MAX	111b (200 mA)
[49:47]	3	Device size multiplier	C_SIZE_MULT	111b(512Bytes)
[46]	1	Erase Single Block Enable	ERASE_BLK_EN	1b
[45:39]	7	Erase Sector Size	SECTOR_SIZE	-- ⁽³⁾
[38:32]	7	Write Protect Group Size	WP_GRP_SIZE	-- ⁽³⁾
[31]	1	Write Protect Group Enable	WP_GRP_ENABLE	1b
[30:29]	2	Reserved	---	00b
[28:26]	3	Write Speed Factor	R2W_FACTOR	010b
[25:22]	4	Max Write Data Block Length	WRITE_BLK_LEN	9h ^{1GB} Ah ^{2GB}
[21]	1	Partial Block Write Allowed	WRITE_BLK_PARTIAL	0b

Bits	Width	Name	Field	Value
[20:16]	5	Reserved	---	0 0000b
[15]	1	File Format Group	FILE_FORMAT_GRP	0b
[14]	1	Copy Flag	COPY	0b
[13]	1	Permanent Write Protection	PERM_WRITE_PROTECT	0b
[12]	1	Temporary Write Protection	TMP_WRITE_PROTECT	0b
[11:10]	2	File Format	FILE_FORMAT	00b
[9:8]	2	Reserved	---	00b
[7:1]	7	CRC	CRC	---
[0]	1	Not used, Always '1'	---	1

- (1) The default value is 32h. The value depends on the Card Type and mode.
 (2) Support command class: 0, 2, 4, 5, 6, 7, and 8. Include: Basic, Block Read/Write, Erase, Write-Protection, Lock Card and Application support. Not supported command class: 1 and 3. Include: Stream Read/ Write.
 (3) This field depends upon the flash used with the controller.

Table 17: Card Specific Data (CSD) Fields (4GB SDHC)

Bits	Width	Name	Field	Value
[127:126]	2	CSD structure	CSD_STRUCTURE	01b
[125:120]	6	reserved	---	---
[119:112]	8	Data read access time 1	TAAC	0Eh
[111:104]	8	Data read access time 2	NSAC	00h
[103:96]	8	max. data transfer rate	TRAN_SPEED	32h ⁽¹⁾
[95:84]	12	Card command classes	CCC	5B5h ⁽²⁾
[83:80]	4	max. read data block length	READ_BL_LEN	9h ⁽³⁾
[79]	1	partial blocks for read allowed	READ_BL_PARTIAL	0b
[78]	1	write block misalignment	WRITE_BLK_MISALING	0b
[77]	1	read block misalignment	READ_BLK_MISALING	0b
[76]	1	DSR implemented	DSR_IMP	0b
[75:70]	6	reserved	---	---
[69:48]	22	device size	C_SIZE	...(4)
[47]	1	reserved	---	---
[46]	1	erase single block enable	ERASE_BLK_EN	1b
[45:39]	7	erase sector size	SECTOR_SIZE	111 1111b
[38:32]	7	write protect group size	WP_GRP_SIZE	000 0000b
[31]	1	write protect group enable	WP_GRP_ENABLE	0b
[30:29]	2	reserved	---	---
[28:26]	3	write speed factor	R2W_FACTOR	010b
[25:22]	4	max. write data block length	WRITE_BL_LEN	9h ⁽³⁾
[21]	1	Partial block for write allowed	WRITE_BL_PARTIAL	0b
[20:16]	5	reserved	---	---
[15]	1	File format group	FILE_FORMAT_GRP	0b
[14]	1	copy flag	COPY	0b
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	0b

Bits	Width	Name	Field	Value
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	0b
[11:10]	2	File format	FILE_FORMAT	00b
[9:8]	2	Reserved	---	---
[7:1]	7	CRC	CRC	---
[0]	1	Not used, always '1'	-	1b

- (1) The default value is 32h. The value depends on the Card Type and mode.
- (2) Support command class: 0, 2, 4, 5, 6, 7, and 8. Include: Basic, Block Read/Write, Erase, Write-Protection, Lock Card and Application support. Not supported command class: 1 and 3. Include: Stream Read/ Write.
- (3) This field is fixed to 9h, which indicates READ_BL_LEN / WRITE_BL_LEN = 512 Byte.
- (4) This field depends upon the flash used with the controller.

10.5 SD Configuration Register (SCR)

The SD Configuration Register (SCR) is 64 bits wide. It is another configuration register. SCR provides information about the SD card's special features that were configured into the given card. The fields for the SDR register are presented in the following table.

Table 18: SD Configuration Register (SCR) Fields

Bits	Width	Name	Field	Value	
[63:60]	4	SCR Structure	SCR_STRUCTURE	0000b	
[59:56]	4	SD Card Spec. Version	SD_SPEC	0010b	
[55]	1	Data Status After Erase	DATA_STAT_AFTER_ERASE	0b	
[54:52]	3	SD Security Support	SD_SECURITY	010b	
[51:48]	4	DAT Bus Width Support	SD_BUS_WIDTHS	0101b	
[47]	1	Spec. version 3.00 or higher	SD_SPEC3	1b	
[46:34]	13	Reserved	--	--	
[33:32]	2	Command support bits	CMD_SUPPORT	1GB/2GB	00b
				4GB	11b
[31:0]	32	Reserved	--	--	

10.6 Operation Condition Register (OCR)

The Operation Condition Register (OCR) register is 32 bits wide. The fields for the OCR register are presented in Table 16.

Table 19: Operation Condition Register (OCR) Fields

Bits	Width	VDD Voltage Window	Value (Binary)				
[0:3]	4	Reserved	0000				
[4]	1	Reserved	0				
[5]	1	Reserved	0				
[6]	1	Reserved	0				
[7]	1	Reserved for Low Voltage Range	0				
[8]	1	Reserved	0				
[9]	1	Reserved	0				
[10]	1	Reserved	0				
[11]	1	Reserved	0				
[12]	1	Reserved	0				
[13]	1	Reserved	0				
[14]	1	Reserved	0				
[15]	1	2.7-2.8	1				
[16]	1	2.8-2.9	1				
[17]	1	2.9-3.0	1				
[18]	1	3.0-3.1	1				
[19]	1	3.1-3.2	1				
[20]	1	3.2-3.3	1				
[21]	1	3.3-3.4	1				
[22]	1	3.4-3.5	1				
[23]	1	3.5-3.6	1				
[24]	1	Switching to 1.8V Accepted (S18A)	-- ⁽³⁾				
[25:29]	5	Reserved	00000				
[30]	1	Card Capacity Status (CCS)	<table border="1"> <tr> <td>1GB/2GB</td> <td>0</td> </tr> <tr> <td>4GB</td> <td>1</td> </tr> </table>	1GB/2GB	0	4GB	1
1GB/2GB	0						
4GB	1						
[31]	1	Card Power Up Status Bit	1 ⁽²⁾				

(1) This bit is valid only when the card power up status bit is set.

(2) This bit is set to LOW if the card has not finished the power up routine.

(3) This bit is set by the host during handshake

10.7 SD Status Register

The SD Status Register (SSR) is 512 bits wide and provides information about the SD card's proprietary features and may be used for application-specific usage. The fields for the SSR register are presented in the following table.

Table 20: SD Status Register (SSR) Fields

Bits	Width	Field	Value	
[511:510]	2	DAT_BUS_WIDTH	10b ⁽¹⁾	
[509]	1	SECURED_MODE	0b	
[508:502]	7	Reserved	--	
[501:496]	6	Reserved	--	
[495:480]	16	SD_CARD_TYPE	0000h	
[479:448]	32	SIZE_OF_PROTECTED_AREA ⁽¹⁾	---	
[447:440]	8	SPEED_CLASS	1GB/2GB	03h
			4GB	04h
[439:432]	8	PERFORMANCE_MOVE	1GB/2GB	03h
			4GB	00h
[431:428]	4	AU_SIZE	9h	
[427:424]	4	Reserved	--	
[423:408]	16	ERASE_SIZE	0200h	
[407:402]	6	ERASE_TIMEOUT	101010b	
[401:400]	2	ERASE_OFFSET	10b	
[399:396]	4	UHS_SPEED_GRADE ⁽²⁾	1GB/2GB	0h
			4GB	Fh
[395:392]	4	UHS_AU_SIZE	9h	
[391:312]	80	Reserved	--	
[311:0]	312	Reserved	Reserved for manufacturer	

(1) Value depends on the Card Type and mode.

(2) Inherent device performance exceeds SD spec. v3.01 UHS Speed Grade 1 criteria.

11. PART NUMBERS

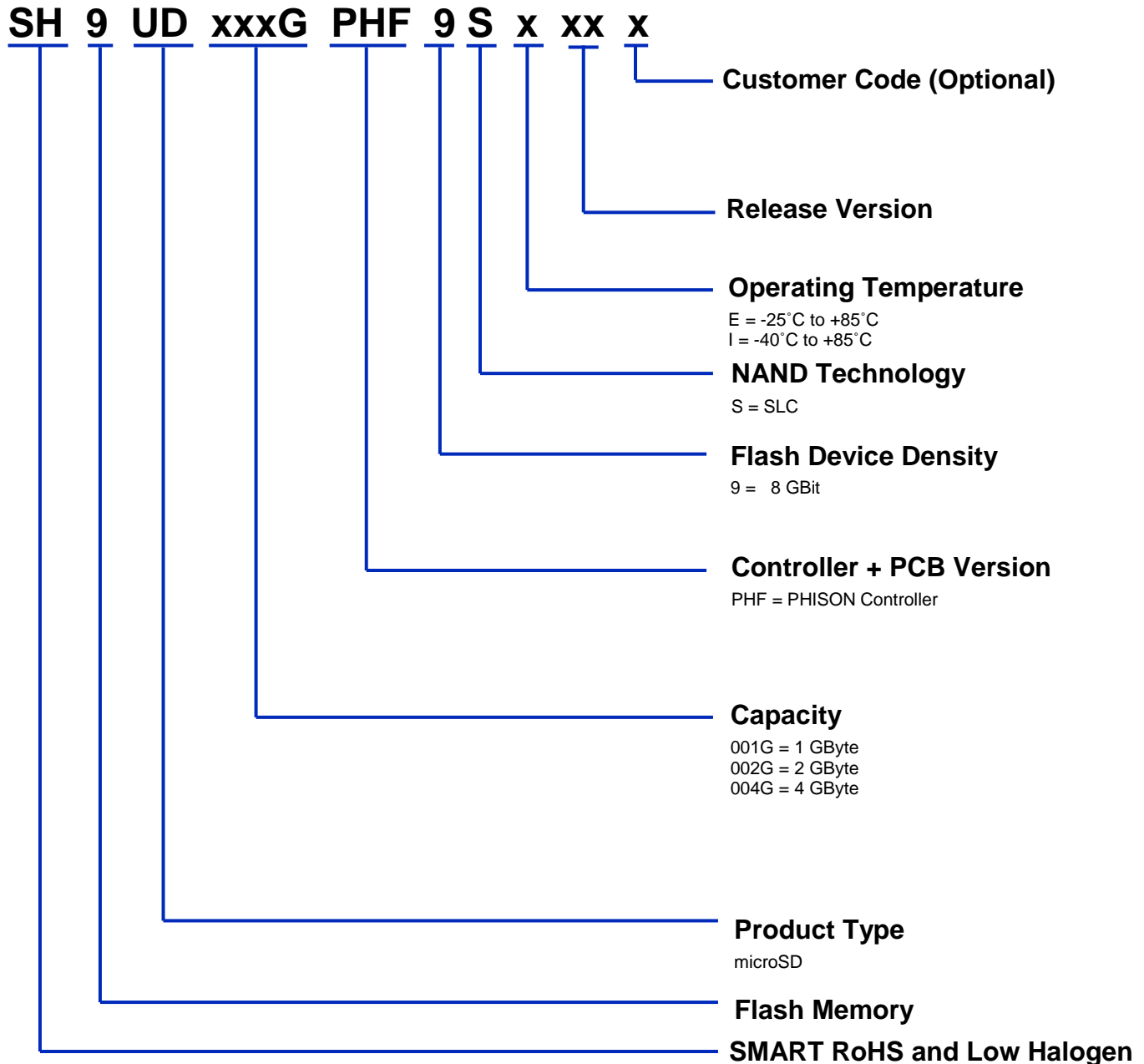
11.1 Part Numbering Information

Table 21: Part Number Information

SMART Part Number	Drive Capacity	Formatted FAT Capacity (Bytes)	Max User Addressable LBA
SH9UD001GPHF9Sx11	1 GB	996,868,096	1,947,008
SH9UD002GPHF9Sx11	2 GB	198,043,2384	3,868,032
SH9UD004GPHF9Sx11	4 GB	3,973,054,464	7,759,872

1. X = E: Extended Temperature Range (-25°C to +85°C)
2. X = I: Industrial Temperature Range (-40°C to +85°C)

11.2 Part Number Decoder



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